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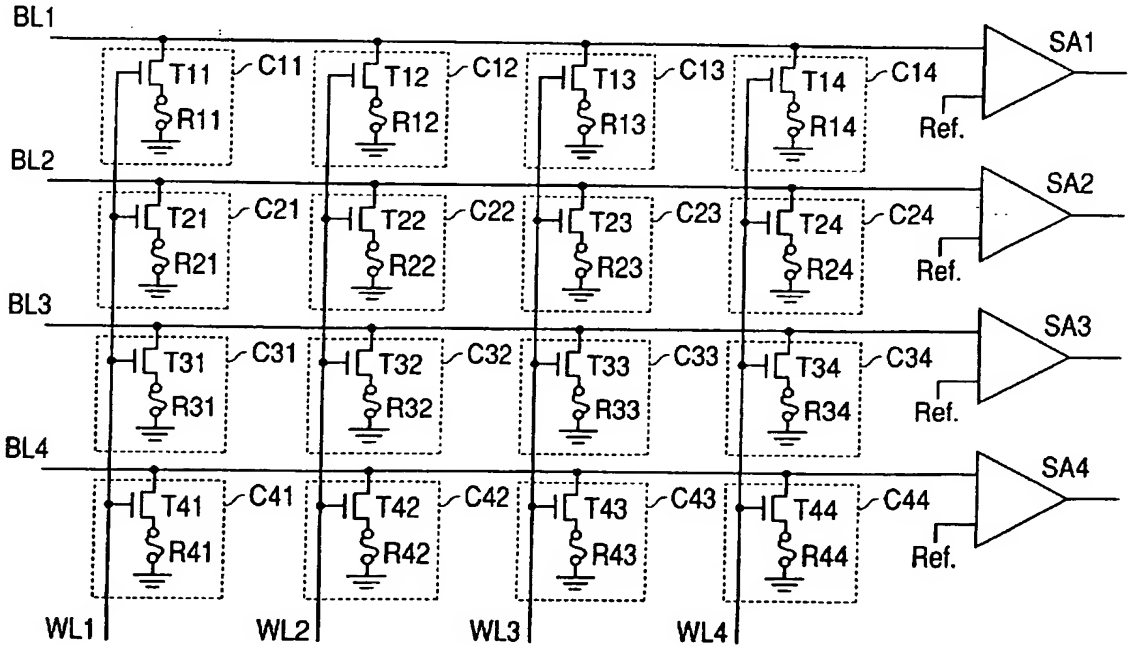
(54) Title: NONVOLATILE MEMORY DEVICE



(57) Abstract: The invention provides a nonvolatile memory device that enables formation of integrated circuits on a substrate such as glass and resin substrates and selection of a desired cell, where the nonvolatile memory device comprises a matrix wiring, a switching element, and a memory element, wherein the memory has a changeable impedance, and both the switching element and the memory element comprises an organic semiconductor or an organic electric conductor or both.

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DESCRIPTION

NONVOLATILE MEMORY DEVICE

TECHNICAL FIELD

The present invention relates to a nonvolatile memory device comprising a matrix wiring, a switching element, and a memory element.

BACKGROUND ART

In recent years, electronic devices exploiting organic semiconductor materials have been developed widely, and many reports have been made on the development of organic EL (Electro-Luminescence), organic TFT (thin film transistor), and organic semiconductor laser. Organic TFT (a type of organic transistor), especially, is promising as a technology to form integrated circuits on a substrate of inexpensive materials such as glass and resins at a low cost.

Regarding the structure of organic transistor, devices including a source electrode, a drain electrode, a gate insulation film and a gate electrode have been proposed (U.S. Patent Nos. 5596208, 6278127, 6326640, 5946551, 5981970, 6210479, 6344660, and 6344662).

As with organic transistors, it is also desired

to construct a nonvolatile memory device on an inexpensive substrate such as glass and resin substrates. Up to now, however, there is no memory structure of which functions are comparable with those of flash memories and EEPROMs (Electrical Erasable Programmable Read Only Memory) fabricated on a silicon substrate. Japanese Patent Application Laid-Open No. 2001-189431 discloses a memory configuration that can store multiple values in a single cell where the impedance of the organic material is changeable by the applied voltage, but it does not disclose such a configuration that an integrated circuit is formed on a glass or resin substrate to select a desired cell.

SUMMARY OF THE INVENTION

The present invention is to solve the problem in memory configuration of conventional technologies, that is, difficulty in forming a nonvolatile memory device on an inexpensive substrate such as glass and resin substrates so as to select desired cells. Accordingly, the object of the present invention is to provide a nonvolatile memory device structured with an organic material, which enables fabrication of an integrated circuit on an inexpensive substrate such as glass and resin substrates to select desired cells.

Thus, according to the present invention, there is provided a nonvolatile memory device that comprises a matrix wiring, a switching element and a memory element, wherein the memory element has a changeable impedance, and both the switching element and memory element contain an organic semiconductor or an organic electric conductor or both.

According to the present invention, a nonvolatile memory device is structured so that it can be formed on a glass or resin substrate and can select a desired cell.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram to show a circuit configuration of the first embodiment;

Fig. 2 is a graph to show the electric characteristics of a memory element;

Fig. 3 is a sectional view showing the relevant parts of a memory device of the first embodiment;

Fig. 4 is a sectional view showing the relevant part of a memory device of the first embodiment;

Fig. 5 is a sectional view showing the relevant parts of a memory device of the first embodiment;

Fig. 6 is a sectional view showing the relevant parts of a memory device of the first embodiment; and

Fig. 7 is a circuit diagram to show the circuit configuration of the second embodiment.

BEST MODE FOR CARRYING OUT THE INVENTION

In the configuration of the nonvolatile memory device of the present invention, the memory element has a changeable impedance, and the switching element and the memory element contains an organic semiconductor or an organic electric conductor or both. This configuration is based on that the impedance of the organic electric conductor in the memory element at a read voltage changes when a write voltage higher than the read voltage is applied.

Particularly, it is preferable that the impedance of the organic electric conductor in the memory element at a read voltage irreversibly increases when a write voltage higher than the read voltage is applied. According to this feature, information once written becomes non-rewritable, which is not only preferable in the viewpoint of security, but also allows use of a simple drive method in comparison with EEPROMs.

The switching element is preferably a transistor including an organic semiconductor or an organic electric conductor. The switching element enables selection of a desired memory cell. The transistor includes field effect-type transistor, thin film-type transistor, junction type transistor, etc. and any of them can be used. An organic semiconductor is a material of which Fermi level is

in the band gap, having semiconductor properties. An organic electric conductor is a material of which Fermi level is near the conduction band, having primarily metallic electric conductivity.

The switching element may be a diode containing an organic semiconductor or an organic electric conductor. In such a case, it is possible to configure a memory device with a relatively simple matrix structure.

It is more preferable to provide ground lines in addition to bit lines and word lines so that one terminal of the transistor is connected to one of the bit lines, another terminal of the transistor is connected to one of the word lines, and still another terminal of the transistor is connected to one of the ground lines through a memory element.

The memory element may be configured to span the gap between two electrodes that are apart in the in-plane direction of the substrate, i.e., a memory element electrode and ground line. This configuration allows formation of a memory element by means of printing or the like.

The nonvolatile memory device is more preferably formed on a resin substrate. This allows use of the nonvolatile memory device in the form of an IC card or IC tag. Such an IC card or IC tag may be used as a nonvolatile memory device for a season

pass, identification card, or package delivery. Alternatively it may be provided on a cartridge to contain a photosensitive drum or a toner in an electro-photography system such as laser beam printers and copy machines, or may be provided on an ink cartridge for ink jet printers of piezo type and bubble jet type. Such use is preferable because the memory device can store various or a large amount of information before shipping or during usage of the product.

Hereinafter, the embodiments of the present invention are described with reference to the drawings.

First embodiment

First, the configuration of the nonvolatile memory device of the embodiment shown in Fig. 1 will be described.

Fig. 1 shows a configuration of a 16 bits memory device consisting of bit lines BL1 to BL4, word lines WL1 to WL4 intersecting with the bit lines, and unit cells C11 to C14, each cell consisting of one of organic TFTs (thin film transistors) T11 to T44 as the switching element containing an organic semiconductor, and one of memory elements R11 to R 44. Each gate electrode of the organic TFT T11 to T44 is connected to a word line, drain electrode to a bit line, source electrode to one terminal of one of the

memory elements R11 to R44 where the other terminal of the memory element is grounded.

A notable structure of the memory element is that an organic electric conductor material is laid between the gap of electrodes. This can be achieved, for an example, by applying a liquid material between electrodes and drying it. Electric characteristics of an example memory element are shown in Fig. 2. When the voltage applied between electrodes is swept from 0 V to 5 V, the characteristics are different between the first and second sweeps. In the first sweep, the amount of current substantially declines around an application voltage of 4 V resulting in a high-resistance state, and this high-resistance state is maintained during the second sweep. This change of resistance is irreversible, and once a high-resistance state is achieved, it never goes back to a low-resistance state. When the read voltage is about 3 V, the resistance of the memory element in the low resistance state increases by two orders in the high-resistance state. That is, the impedance increases irreversibly.

Examples of the organic electric conductors having the above-described characteristics include polythiophen derivatives, polypyrrole derivatives, polyaniline derivatives, and poly-para-phenylenevinylene derivatives.

Next, the driving method of the present memory device will be described with reference to an example.

First, the read operation will be explained. It is supposed that each TFT acts as a p-channel. As a reference voltage ("Ref." in Fig. 1), a voltage of -2 V (corresponds to 2/3 of the power supply voltage 3 V) is applied to a sense amplifier. Next, information in the cell C23 is read as follows. A voltage of -3 V is applied to the word line WL3 turning the selected transistor T23 to ON state. Then a constant current of several μA is applied to the bit line BL2 with a voltage limit of -3 V. At this moment, if C23 is selected and R23 is in a low-resistance state, the current flows from BL2 to T23 and to the ground, and the potential of the BL2 becomes close to the ground voltage. Thus, the potential of the bit line BL2 becomes higher than the reference voltage and the sense amplifier SA2 outputs "1". On the other hand, when R23 is in a high-resistance state, the current hardly flows from BL2 to T23 and to the ground and the potential of BL2 becomes close to the power supply voltage. Thus the potential of the bit line BL2 becomes lower than the reference voltage and the sense amplifier SA2 outputs "0".

Next, write operation will be described. Suppose that R23 is in a low-resistance state as the

initial state. The word line WL3 is applied a voltage of -3 V and the selected transistor T23 is turned ON. Then, a constant current of about 10 μA is applied to the bit line BL2 with a voltage limit of -6 V. At this point, C23 is selected and a voltage of higher than 5 V is applied to R23, a current of 10 μA flows. At this moment, R23 transforms into a high-resistance state irreversibly. By this action, information is written into C23.

First embodiment

Next, a manufacturing process of a memory device will be described to explain the present embodiment.

Figs. 3 to 6 are schematic diagrams to explain the fabrication process of the memory device of the present embodiment. Numeral 1 denotes a substrate, 2: contact, 3: memory element electrode, 4: ground line, 5: gate electrode, 6: gate insulation film, 7: drain electrode, 8: source electrode, 9: organic semiconductor layer, 10: protection film, 11: organic electroconductive material for memory element, and 12: protection film.

First, as shown in Fig. 3, the memory electrode 3, the ground line 4, and the gate electrode 5 are formed by etching a copper film provided on the both faces (back and front faces) of the substrate 1 made of epoxy resin, and the contact 2 is formed filling a

through-hole by copper plating. Here the gate electrode 5 is connected to the word line. On one face of the substrate 1, the memory element 3 and the ground line 4 are provided, and the gate electrode 5 is provided on the other face.

Next, as shown in Fig. 4, an aluminum oxide thin film is formed as the gate insulation film 6 by a spattering method. The gate insulation film is selectively formed using a metal mask so as to cover the gate electrode 5. Further, a gold thin film is formed as the drain electrode 7 and the source electrode 8 by a vacuum deposition method. They are selectively formed using a metal mask as with the gate insulation film 6. At this moment, the drain electrode 7 is connected to the bit line, and the source electrode 8 is connected to the contact 2.

Next, as shown in Fig. 5, pentacene is vacuum-deposited as the organic semiconductor layer 9. As with the gate insulation film 6, the organic semiconductor layer 9 is selectively formed using a metal mask so as to cover the region between the source electrode 8 and the drain electrode 7 including a part of each electrode, that is, to cover the region between the electrodes. Next, novolac resin is applied and cured as the protection film 10.

Next, as shown in Fig. 6, organic electric conductor PEDOT/PSS (Polyethylene-dioxy-

thiophen/polystyrene sulfonic acid) (Reference numeral 11) is applied and dried so as to span the gap between the memory element electrode 3 and the ground line 4, specifically to cover the region between the memory element electrode 3 and the ground line and part of each of them thereby forming the memory element. After that, a protection film 12 is formed thereon.

Moreover, though it is not shown in the drawing, the bit line is connected to one terminal of the sense amplifier and outputs "1" when the bit line potential is higher than the reference voltage comparing with the reference voltage of the other terminal (high potential: a voltage close to the ground voltage), and outputs "0" when the bit line potential is lower than the reference potential (low potential: a voltage close to the source voltage).

Driving of the thus fabricated memory device will be described on the precondition that a read operation is -3V and a write operation is -6V.

First, read operation will be described. A voltage of -2 V (that is 2/3 of the power source voltage 2 V) is applied to the sense amplifier as the reference voltage ("Ref." in Fig. 1).

Next, operation of reading the information in the cell C23 is conducted. A voltage of -3V is applied to the word line WL3, and the selected

transistor T23 is turned ON. Next, a current of 5 μA is supplied to the bit line BL2 with a voltage limit of -3 V. At this moment, when C23 is selected and R23 is in a low-resistance state, the current flows from BL2 to T23, and to the ground causing the BL2 potential to become close to the ground voltage. Therefore, the potential of the bit line BL2 becomes higher than the reference voltage and the sense amplifier SA2 outputs "1". On the other hand, when R23 is in a high-resistance state, the current flowing from BL2 to T23, and to the ground becomes scarce, and the potential of BL2 becomes close to the power source voltage. Therefore, the potential of the bit line BL2 becomes lower than the reference voltage and the sense amplifier SA2 outputs "0".

Next, write operation will be described. Suppose that R23 is in a low-resistance state as the initial state. A voltage of -3 V is applied to the word line WL3 and selected transistor T23 is turned "ON". Then a constant current of 10 μA is applied to the bit line BL2 with a voltage limit of -6 V. At this moment, if C23 is selected, a voltage higher than 5 V is applied to R23, and a current of 10 μA flows. At this moment, R23 transforms into a high-resistance state irreversibly. As such, information is written into C23.

In the nonvolatile memory device of the present

invention, the switching element may be a diode. Alternatively, the nonvolatile memory device of the present invention may use a junction type transistor as the switching element.

Second embodiment

The nonvolatile memory device of this embodiment uses a diode as the switching element. Fig. 7 shows an example of the configuration of this embodiment.

In the present embodiment, as with the first embodiment, each cell has a switching element and a memory element. In the first embodiment, each cell has a transistor element as the switching element, instead, each cell has a diode element in the second embodiment as the switching element.

As shown in Fig. 7, the nonvolatile memory device of this embodiment has a plurality of such cells in the row and column directions (from C11 to C44). Taking one cell, for example, the cell C11 has the diode D11 and the memory element M11. Each memory element is connected on one end to the diode of each cell, and the other end is commonly connected to a word line WL. There are multiple word lines WL, and each of them is connected to a plurality of memory elements on a column-by-column base. One end of the diode that is not connected to the memory element is commonly connected to one of the bit lines

BL. There are multiple bit lines BL and each of them is connected to one end of a plurality of diodes on a row-by-row base.

Next, read operation will be described. For example, selecting the cell C22, a constant voltage Vcc is applied to BL2 so that current flows to the grounded BL2 via the resistance R2. In this occasion, to word lines WL other than WL2, a voltage of not lower than Vcc is applied so that no current will flow in cells except selected one. At this moment, by comparing the potential of BL2 with the reference voltage Ref., it is possible to read information.

Next, write operation will be described. For example, selecting the cell C22, a constant voltage 2Vcc is applied to BL2 so that current flows to BL2 via R2. In this occasion, to word lines WL other than WL2, a voltage not lower than 2Vcc is applied so that current will not flow to cells except selected ones. This arrangement causes the memory element D22 of the selected C22 to be applied a large voltage and thereby the impedance will change.

CLAIMS

1. A nonvolatile memory device comprising a matrix wiring, a switching element and a memory element,

wherein the memory element has a changeable impedance, both the switching element and memory element contains an organic semiconductor element or an organic electric conductor or both.

2. The nonvolatile memory device according to claim 1, wherein the memory element contains an organic electric conductor of which impedance changes according to an applied write voltage, the write voltage being higher than a read voltage.

3. The nonvolatile memory device according to claim 1, wherein the memory element contains an organic electric conductor of which impedance changes irreversibly according to an applied write voltage, the write voltage being higher than a read voltage.

4. The nonvolatile memory device according to claim 1, wherein the switching element is a transistor.

5. The nonvolatile memory device according to

claim 1, wherein the switching element is a diode.

6. The nonvolatile memory device according to claim 4, wherein the matrix wiring comprises bit lines, word lines and ground lines, one terminal of the transistor is connected to one of the bit lines, another terminal of the transistor is connected to one of the word lines, and still another terminal of the transistor is connected to one of the ground lines via the memory element.

7. The nonvolatile memory device according to claim 1, wherein the memory element has a structure for connecting two electrodes which are apart in the in-plane direction of the substrate.

8. The nonvolatile memory device according to claim 1, wherein the matrix wiring, the switching element, and the memory element are formed on a resin or glass substrate.

9. An IC card or IC tag comprising a nonvolatile memory device according to claim 8.

10. An IC tag comprising the nonvolatile memory device according to claim 1.

11. A cartridge for an image-forming apparatus based on an electronic photograph scheme comprising either the IC card or the IC tag according to claim 9.

12. A cartridge for an ink-jet printer comprising either the IC card or the IC tag according to claim 9.

FIG. 1

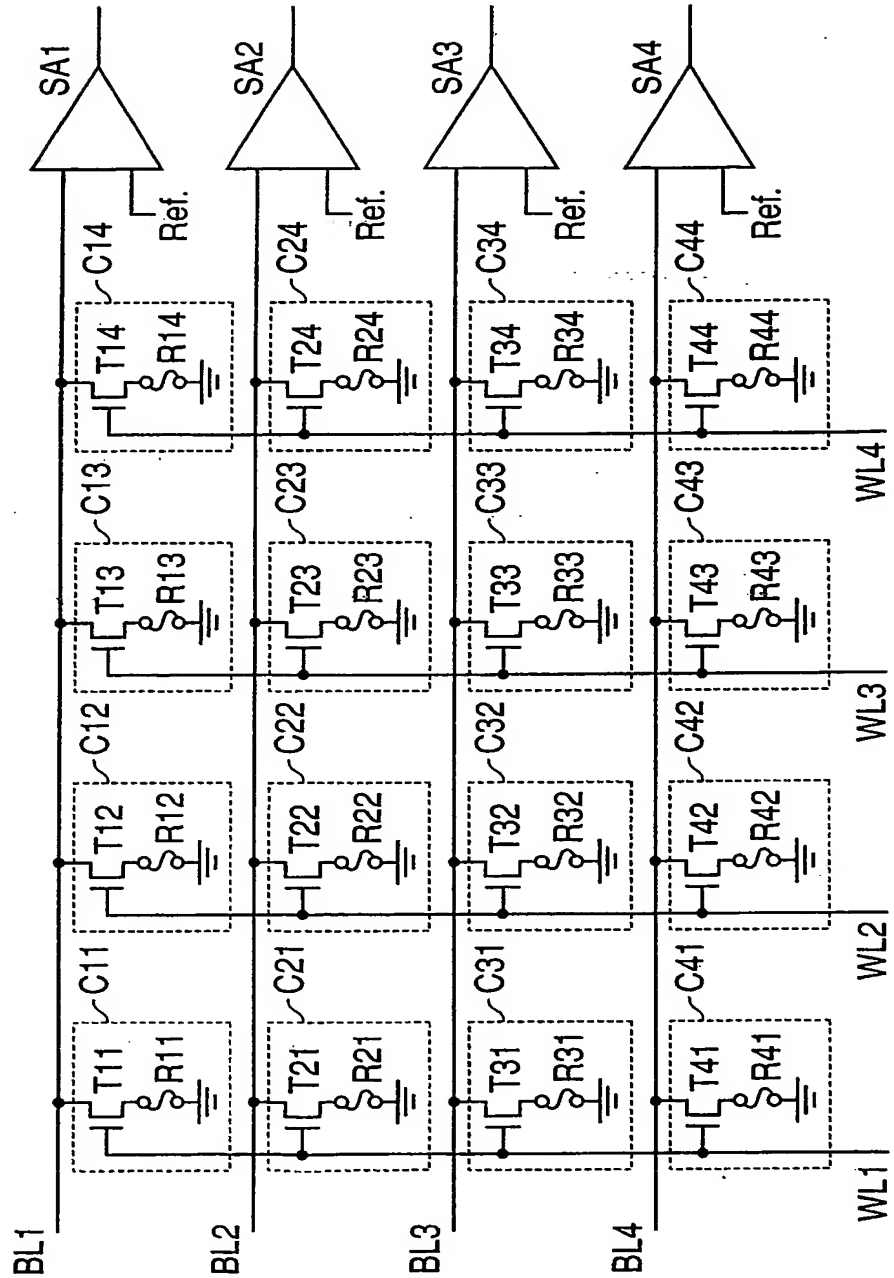


FIG. 2

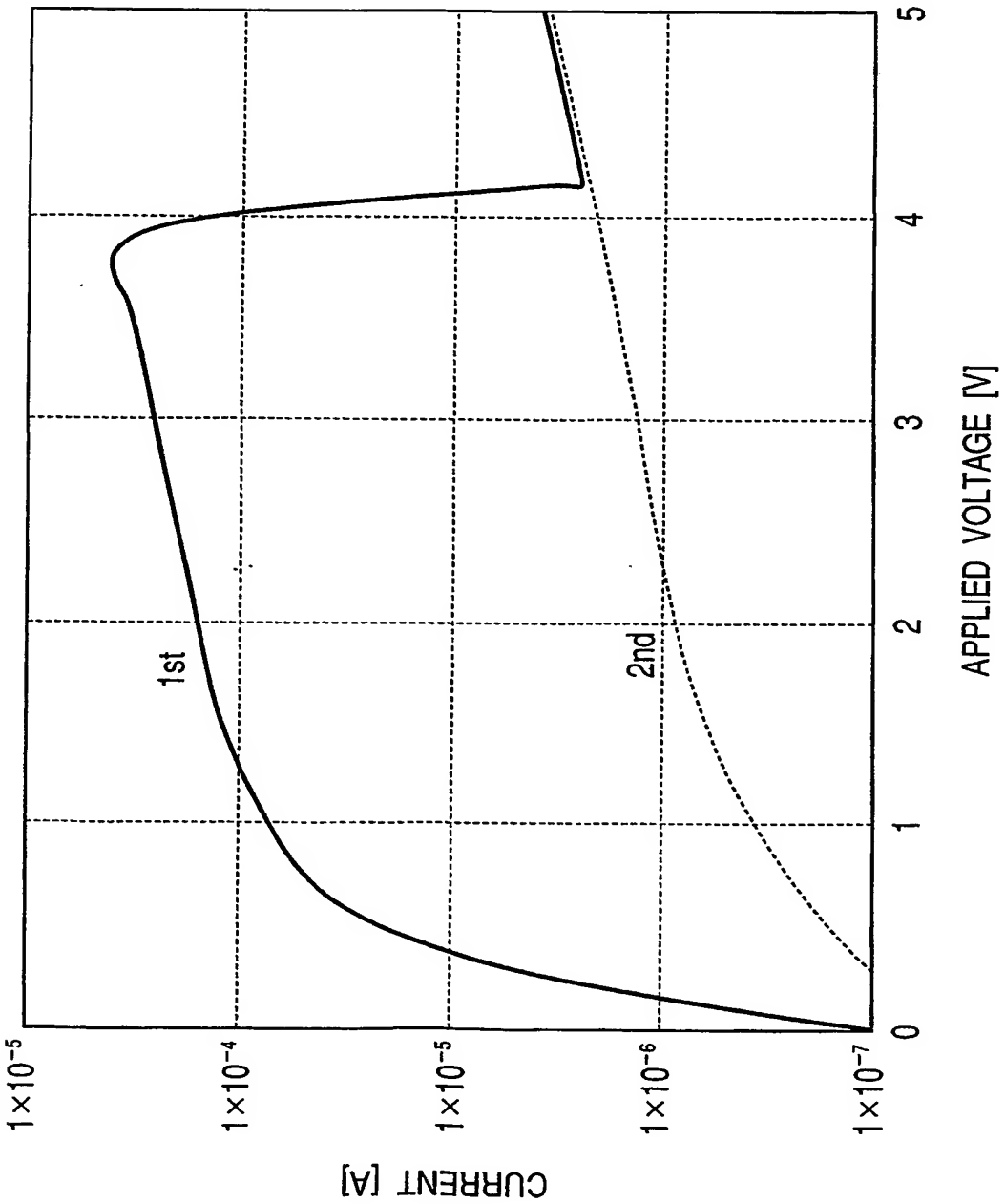


FIG. 3

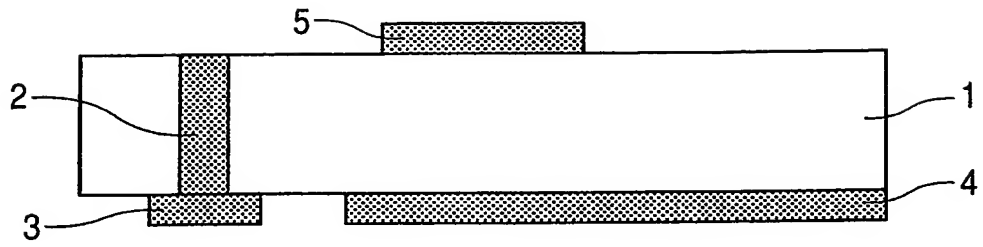


FIG. 4

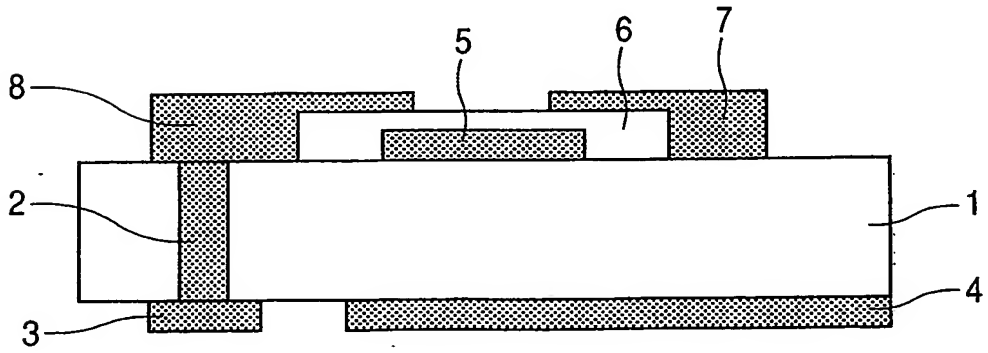


FIG. 5

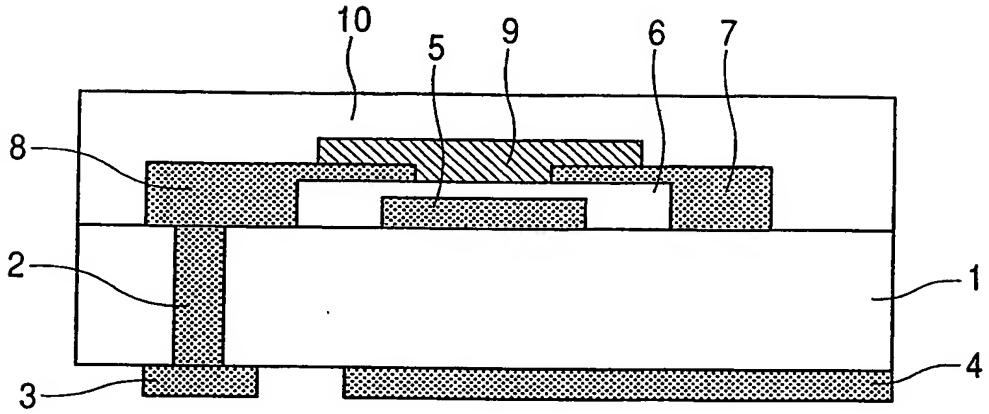


FIG. 6

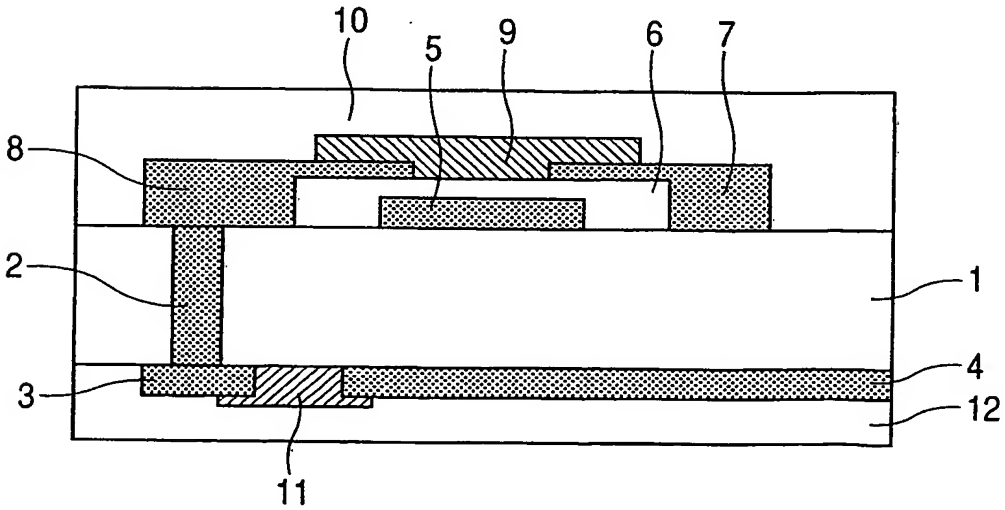
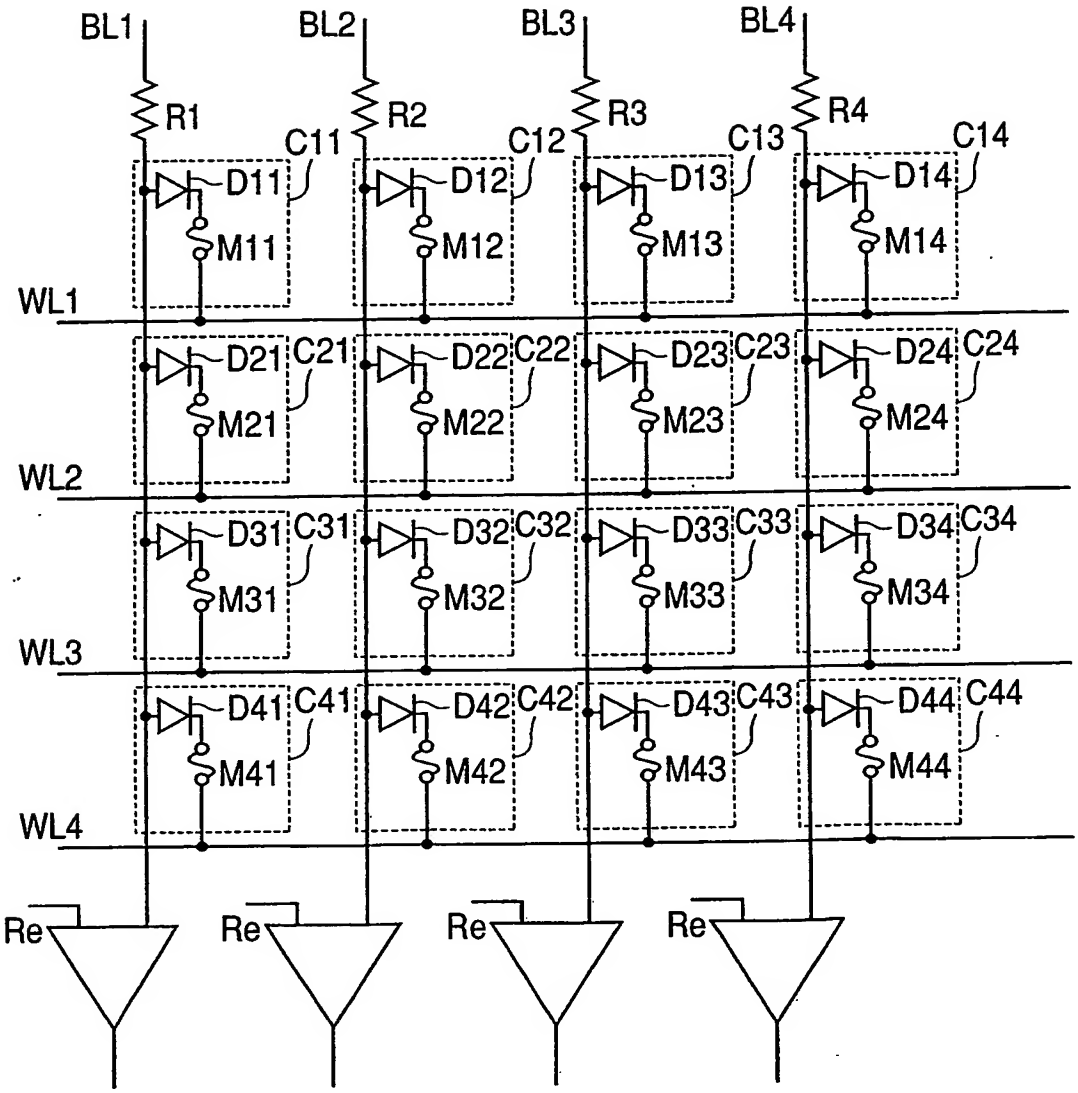


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10017

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H01L27/10 H01L51/00 G11C13/02 G06K19/077

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H01L27/10 H01L51/00 G11C13/02 G06K19/077 H01L29/786 H01L21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Japanese Utility Model Gazette 1922-1996, Japanese Publication of Unexamined Utility Model Applications 1971-2003, Japanese Registered Utility Model Gazette 1994-2003, Japanese Gazette Containing the Utility Model 1996-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 01/73845 A1(KONINKLIJKE PHILIPS ELECTRONICS N.V.) 2001.10.04 a whole document, figures 1-3 a whole document, figures 1-3 & JP 2003-529223 A, a whole document, figures 1-3 & US 2001/0045593 A1 & EP 1186042 A1 & KR 2002030272 A & CN 1381071 A	1-3,5,7,8 4,6,9-12
Y	US 5625219 A(KABUSHIKI KAISHA TOSHIBA) 1997.04.29 a whole document, figure 12 & JP 6-302775 A, a whole document, figure 11 & KR 157673 B1	4,6
Y	JP 7-176703 A(OHMI TADAHIRO) 1995.07.14 [0030], figure 3. & WO 95/17009 A1	4,6

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
14.10.03	28.10.03

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP03/10017

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6385407 B1(HITACHI MAXELL, LTD.) 2002.05.07 a whole document, figures 1-9 & JP 2000-246921 A, a whole document, figures 1-9	9-12

Form PCT/ISA/210 (continuation of second sheet) (July 1998)